REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 13 and 19-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Shimoji (U.S. Patent No. 5,463,579). Applicant respectfully traverses this rejection and submits that claims 13 and 19-20 are allowable for at least the following reasons.

The Applicant respectfully maintains that Shimoji does not disclose a floating gate structure that is spaced apart from the source/drain/channel regions in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second section by a second distance, wherein the first distance is less than the second distance. Applicant notes that the floating gate structure of Shimoji only partially covers the source/drain/channel region and that for this partial coverage the spacing of Shimoji's floating gate structure from the source/drain/channel region is uniform. Shimoji discloses a split gate memory cell with a single FET that has a floating gate that only partially covers a channel region, and a single control gate that covers the floating gate and the remaining portion of the channel region, allowing the split gate memory cell to function as a series coupled memory cell and access gate. *See, e.g.*, Shimoji, Figs. 1 and 5, Abstract, column 2, line 65 to column 3, line 15, column 3, line 62 to column 4, line 42. The Applicant therefore respectfully maintains that Shimoji does not teach or suggest a memory cell having a floating gate structure that is spaced apart from the source/drain/channel regions in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second section by a second distance, wherein the first distance is less than the second distance.

Claim 13 recites, in part, "each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance." As stated above, Shimoji does not teach or suggest a memory cell having a first and second adjacent field effect transistors (FETs) having a common floating gate. Therefore, Shimoji does not teach or suggest all elements of claim 13.

Applicant respectfully contends that claim 13 has been shown to be patentably distinct from the cited reference. As claims 19-20 depend directly or indirectly from independent claim

13, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 13 and 19-20.

Claims 13 and 19-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ozawa (U.S. Patent No. 5,461,249). Applicant respectfully traverses this rejection and submits that claims 13 and 19-21 are allowable for at least the following reasons.

The Applicant respectfully maintains that Ozawa also does not disclose a floating gate structure that is spaced apart from the source/drain/channel regions in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second section by a second distance, wherein the first distance is less than the second distance. Applicant further maintains that Ozawa also discloses a split gate memory cell that has a floating gate that only partially covers a channel region, and a single control gate that covers the floating gate and the remaining portion of the channel region, allowing the split gate memory cell to function as a series coupled memory cell and access gate. *See, e.g.*, Ozawa, Figs. 2 and 3, Abstract, column 2, lines 22-39, column 5, lines 16-42. The Applicant therefore respectfully maintains that Ozawa does not teach or suggest a memory cell having a first and second adjacent field effect transistors (FETs), each FET with its own channel, source, and drain regions, but having a common floating gate.

Claim 13 recites, in part, "each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance." As stated above, Ozawa does not teach or suggest a memory cell having a first and second adjacent field effect transistors (FETs) having a common floating gate. Therefore, Ozawa does not teach or suggest all elements of claim 13.

Applicant respectfully contends that claim 13 has been shown to be patentably distinct from the cited reference. As claims 19-21 depend directly or indirectly from independent claim 13, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 13 and 19-21.

Claims 13, 16 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by Guterman et al. (U.S. Patent No. 2004/0063283). Applicant respectfully traverses this rejection. Applicant reserves the right to swear behind the reference Guterman et al., but submits that claims 13, 16 and 17 are allowable for the following reasons.

The Applicant respectfully maintains that Guterman et al. also does not disclose a floating gate structure that is spaced apart from the source/drain/channel regions in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second section by a second distance, wherein the first distance is less than the second distance. Applicant maintains that Guterman et al. also discloses a variation of a split gate memory cell that has a floating gate (107) that only partially covers a channel region (106), and two control gates. The first control gate (108) covers only the floating gate (107), the second control gate (109) fully covers the floating gate (107), first control gate (109) and the remaining portion of the channel region (106-1), allowing the memory cell to function as a series coupled memory cell and access gate (Fig. 1C). *See, e.g.*, Guterman et al., Figs. 1A-1D, Page 3, paragraph 0052, Page 5, paragraph 0063. The Applicant therefore respectfully maintains that Guterman et al. does not teach or suggest a memory cell having a first and second adjacent field effect transistors (FETs), each FET with its own channel, source, and drain regions, but having a common floating gate.

Claim 13 recites, in part, "each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance." As stated above, Guterman et al. does not teach or suggest a memory cell having a first and second adjacent field effect transistors (FETs) having a common floating gate. Therefore, Guterman et al. does not teach or suggest all elements of claim 13.

Applicant respectfully contends that claim 13 has been shown to be patentably distinct from the cited reference. As claims 16 and 17 depend directly or indirectly from independent claim 13, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 13, 16 and 17.

Claim Rejections Under 35 U.S.C. § 103

Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Guterman et al. (U.S. Patent No.2004/0063283). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant submits that claim 18 is allowable for the following reasons.

As stated above in response to the rejection under 35 U.S.C. § 102(e) of claim 13, which claim 18 depends from, Guterman et al. fails to teach or suggest a memory cell having a first and second adjacent field effect transistors (FETs), each FET with its own channel, source, and drain regions, but having a common floating gate. Therefore, Guterman et al. does not teach or suggest all elements of independent claim 13 and therefore does not teach or suggest all elements of claim 18.

Applicant respectfully contends that claim 18 has been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 18.

Objected Claims

Claims 14 and 15 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicant has amended claim 14 to include the limitations of rejected base claim 13 as suggested by the Examiner. As claim 15 depends from and further defines amended claim 14, it is also deemed to be in condition for allowance. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claims 14 and 15.

Allowable Subject Matter

Claims 1-12 and 22-32 were indicated to be allowable by the Examiner.

CONCLUSION

Claim 14 was amended. Claims 1-32 are currently pending. Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of claims 1-32.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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